

Art Unit 2186  
Serial No. 10/676,739

Reply to Office Action of: October 25, 2005  
Attorney Docket No.: K35A1281

### REMARKS

The Applicants thank the Examiner for his careful and thoughtful examination of the present application. By way of summary, Claims 1-20 were pending in this application. In the present amendment, the Applicants have canceled Claims 2, 15 and 20 without prejudice or disclaimer and amended Claims 1, 3, 6, 14, 16 and 18. Accordingly, Claims 1, 3-14 and 16-19 remain pending for consideration.

### AMENDMENTS TO THE CLAIMS

Claim 1 has been amended to clarify the claim language, and to incorporate limitations from previously pending Claim 2. Claim 3 has been amended to depend properly from Claim 1. Claim 6 has been amended to clarify the claim language. Claim 14 has been amended to clarify the claim language, and to incorporate limitations from previously pending Claim 15. Claim 16 has been amended to depend properly from Claim 14. Claim 18 has been amended to clarify the claim language. The amendments to these claims have not been made for the purposes of patentability, and it is believed that the claims would satisfy the statutory requirements for patentability without the entry of such amendments

### REJECTION UNDER 35 USC § 102(b)

The Office action rejected Claims 1-2, 4-15 and 17-19 under 35 U.S.C. § 102(b) as being anticipated by U.S. patent no. 6,360,299, issued to Arimilli *et al.* (the Arimilli patent). The Applicants respectfully traverse this rejection because the Arimilli patent fails to identically teach every element of the claims. See M.P.E.P. § 2131 (stating that in order to anticipate a claim, a prior art reference must identically teach every element of the claim).

In particular, amended Claim 1 recites a method for reducing micro-controller access time, comprising: "if the current requested data resides in a first line-cache segment of a first segment-group: providing the current requested data to the micro-controller; and automatically filling a second line-cache segment of the first segment-

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group with data retrieved from the remote memory wherein the retrieved data is sequential in the remote memory to the provided current requested data if the second line-cache segment hosted a most-recently requested data prior to the current requested data." These limitations of Claim 1 are not taught or suggested by Arimilli.

The Examiner asserts that Arimilli teaches to "automatically fill a subsequent second segment . . . which was most recently previously accessed relative to the most current request with corresponding sequentially accessed data (column 10 lines 27-28)." Office action, page 2. The Applicants respectfully disagree.

The Applicants submit that column 10, lines 27-31 recites: "[a]n additional bit 229 may optionally be utilized to indicate as between the two slots, which is the most recently used, for those cases wherein a prefetch request misses the L2 cache and both slots already have prefetched lines with different stream IDs." However, this passage does not teach the step of "automatically filling a second line-cache segment . . . if the second line-cache segment hosted a most-recently requested data," as recited by the amended claim.

Instead, Arimilli's method of selecting a next "victim" line for filling uses "a standard victim selection algorithm, such as a least-recently, or less-recently, used (LRU) algorithm, which is applied to all sets including the prefetched line." Col. 9, ll. 55-58. Thus, according to Arimilli's method, the line that has been least-recently used is used to receive new data. For example, Arimilli describes that "[w]hen a prefetch request misses the L2 cache and neither slot is allocated, a victim is selected using the standard LRU algorithm" (Col. 10, ll. 4-6), and "[t]he prefetch slots are not exclusively used for speculative requests; they may be used for non-prefetch requests if the standard LRU algorithm were to select[] that set for victimization" (Col. 10, ll. 11-14). Arimilli does not disclose any other algorithm for selecting the next line for victimization. Therefore, Arimilli does not disclose "automatically filling a second line-cache segment . . . if the second line-cache segment hosted a most-recently requested data." Instead, the additional bit 229 called out by the Examiner would likely be used to protect a slot, by preventing the most recently used slot from being victimized. Indeed, there is no

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disclosure or suggestion anywhere in Arimilli of automatically filling a line-cache segment if the most recently used bit 229 is set for that line-cache segment.

For at least these reasons, Applicants respectfully submit that the rejection of amended Claim 1 over Arimilli is improper, and the Applicants respectfully request allowance of Claim 1.

Claims 4-13, which depend from Claim 1, are believed to be patentable for at least the same reasons articulated above with respect to Claim 1, and because of the additional features recited therein.

Amended Claim 14 similarly recites a disk drive control system comprising a micro-controller cache system adapted to: "if the current requested data resides in a first line-cache segment of a first segment-group . . . automatically fill a second line-cache segment of the first segment-group with data retrieved from the remote memory wherein the retrieved data is sequential in the remote memory to the provided current requested data if the second line-cache segment hosted a most-recently requested data prior to the current requested data." These limitations of Claim 14 are not taught or suggested by Arimilli.

As discussed above, Arimilli does not teach a micro-controller cache system adapted to "automatically fill a second line-cache segment . . . if the second line-cache segment hosted a most-recently requested data," as recited by the claim. Therefore, for reasons similar to those discussed above, Applicants respectfully submit that the rejection of amended Claim 14 over Arimilli is improper, and the Applicants respectfully request allowance of Claim 14.

Claims 17-19, which depend from Claim 14, are believed to be patentable for at least the same reasons articulated above with respect to Claim 14, and because of the additional features recited therein.

#### REJECTION UNDER 35 USC § 103(a)

The Office action further rejected Claims 3 and 16 under 35 U.S.C. § 103(a) as being unpatentable over the Arimilli patent in view of U.S. patent no. 5,345,560, issued to Miura *et al.* (the Miura patent). The Applicants respectfully traverse this rejection

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because the Arimilli patent, alone or in combination with the Miura patent, fails to teach or suggest the elements of the claims. See M.P.E.P. § 2143 (stating that in order to establish a *prima facie* case of obviousness for a claim, the prior art references must teach or suggest all the claim limitations).

In particular, the Miura patent does not cure the deficiencies of the Arimilli patent discussed at length above with respect to Claims 1 and 14. Therefore, for reasons similar to those discussed above, Applicants respectfully submit that amended Claims 1 and 14 are not obvious in view of the Arimilli and Miura patents.

Claims 3 and 16, which depend from Claims 1 and 14 respectively, are believed to be patentable for at least the same reasons articulated above with respect to Claims 1 and 14, and because of the additional features recited therein.

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### CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully submit that the pending claims are now in condition for allowance and request reconsideration of the rejections. If it is believed that a telephone conversation would expedite the prosecution of the present application, or clarify matters with regard to its allowance, the Examiner is invited to contact the undersigned attorney at the number listed below.

No fee is believed to be due. However, the Commissioner is hereby authorized to charge payment of any required fees associated with this Communication or credit any overpayment to Deposit Account No. 23-1209.

Respectfully submitted,

Date: March 23, 2006

By: 

Jason T. Evans, Esq.  
Reg. No. 57,862

WESTERN DIGITAL TECHNOLOGIES, INC.  
20511 Lake Forest Drive  
Lake Forest, CA 92630  
Tel.: (949) 672-7000  
Fax: (949) 672-6604